VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at line 8 of page 2 has been amended as follows:

Burst mode memory devices initially operated by serially accessing the memory cells in an active row. However, with the advent of synchronous DRAM ("SDRAMs") having two separately addressable arrays of memory cells, interleave memory accesses were introduced. In interleave memory accesses, the memory addresses increment by toggling the least significant bit ("LSB") every address, toggling the next to least significant bit ("NLSB") every other address, toggling the next most significant bit every fourth address, etc. To further increase memory access speeds, a 2-bit prefetch mode of operation was developed. In the 2-bit prefetch mode of operation, the LSB of an address is ignored, and corresponding columns in respective arrays are thus simultaneously accessed using the address designated by all but the LSB of the column address. The column that is accessed in each array is thus designated by the [NLSB]NLS and higher bits and, as a practical matter, should be the same for both arrays so that corresponding columns in both arrays are simultaneously accessed.

Paragraph beginning at line 1 of page 3 has been amended as follows:

The sequence of column addresses that should be generated starting at an initial, externally applied column address of "CA_N...CA_2, CA_1, CA_0" (where "CA_0" is the LSB, "CA_1" is the NLSB, and "CA_N...CA_2" are higher order bits) are shown below (ignoring the bits that are higher order than CA_3). The address sequence for an interleave mode with a starting column address of "0 1 1 0" is as follows:

"0 1 1 0" (starting column address)

"[0 1 1 1]0 1 1 1"

"[1 0 0 0]0 1 0 0"

"[1 0 0 1]0 1 0 1"

"[1 0 1 0]0 0 1 0"

"[1 0 1 1]0 0 1 1"

"[1 1 0 0]0 0 0 0"

"[1 1 0 1]0 0 0 1"

Paragraph beginning at line 14 of page 3 has been amended as follows:

The address sequence for an interleave mode with a starting column address of "0 1 0 1" is as follows:

"0 1 0 1" (starting column address)

"0 1 0 0"

"0 1 1 1"

"0 1 1 0"

"[1 0 0 1]0 0 0 1"

"[1 0 0 0]0 0 0 0"

"[1 0 1 1]0 0 1 1"

"[1 0 1 0]0 0 1 0"

Paragraph beginning at line 24 of page 3 has been amended as follows:

The address sequence for a serial mode with a starting column address of "0 1 1 0" is as follows:

"0 1 1 0" (starting column address)

"0 1 1 1"

"[1 0 0 0]0 0 0 0"

"[1 0 0 1']0 0 0 1"

"[1 0 1 0']0 0 1 0"

"[1 0 1 1']0 0 1 1"

"[1 1 0 0']0 1 0 0"

"[1 1 0 1]0 1 0 1"

Paragraph beginning at line 4 of page 4 has been amended as follows:

In all cases, the LSB in all of the above examples is ignored by the memory devices, as previously explained. In each of the above examples, the [NLSB]NLS and higher bits select [selects]the same column in each pair of addresses, and the LSB[, which is ignored in the SDRAM,] is effectively "0" for the even array and "1" for the odd array. For example, the first pair of column addresses in the interleave mode with a starting column address of "0 1 1 0" selects a column in both arrays having a NLSB (*i.e.*, an effective LSB) of "1", and the second pair of column addresses selects a column in both arrays having a NLSB (*i.e.*, an effective LSB) of "0."

Paragraph beginning at line 12 of page 4 has been amended as follows:

In all of the above cases, the sequence of column addresses can be generated by an incrementing a [bust]burst counter that generates only the NLSB and all bits more significant than the NLSB since the LSB is ignored by [a memory device and]the counter . Note, however, a problem that develops in the serial mode where the starting column address is "0 1 0 1":

"0 1 0 1" (starting column address)

"0 1 1 0"

"0 1 1 1"

"1 0 0 0"

"1 0 0 1"

"1 0 1 0"

"1 0 1 1"

"1 1 0 0"

Paragraph beginning at line 16 of page 5 has been amended as follows:

The above address sequence cannot be generated by [incrementing]a serial increment of a burst counter since the addresses in the above sequence (again, ignoring the LSB) do not increment. Thus, an interleave sequence for certain starting addresses cannot be generated in the 2-bit prefetch mode by simply incrementing a burst counter.

Paragraph beginning at line 20 of page 5 has been amended as follows:

Conventional burst mode 2-bit prefetch memory devices capable of operating in either a serial mode or an interleave mode generally require two different [bust]burst mode counters, one of which is used in the serial mode and the other of which is used in the interleave mode. The need for separate burst accessing circuitry for each of these two burst modes significantly increases the cost of memory devices operating in these two modes.

Paragraph beginning at line 14 of page 7 has been amended as follows:

After the row address has been applied to the address register 12 and stored in one of the row address latches 26, a column address is applied to the address register 12. The address register 12 couples the column address to a column address latch 40. Depending on the operating mode of the SDRAM 10, the column address is used for either of two purposes. First, in a normal operating mode, the column address is coupled through a burst counter 42 to a column address buffer 44 to select a column of memory cells in one or both of the memory arrays 20, 22. Second, in a burst operating mode, the column address is coupled to the burst counter 42 and used as a starting column address ("SCA"). The [bust]burst counter then generates a sequence of column addresses starting at the SCA, and applies the sequence of column addresses to the column address buffer 44. In either case, the column address buffer 44 applies a column address to a column decoder 48a,b for each array 20, 22. The column decoders

48a,b apply respective decoded column addresses to respective sense amplifiers and associated column circuitry 50, 52 for the respective arrays 20, 22.

Paragraph beginning at line 13 of page 9 has been amended as follows:

For example, in the serial mode using the above example of a starting column address of "0 1 0 1" the correct sequence is:

"1 1 0 1" (starting column address)
"1 1 0 0"
"1 0 1 1"
"1 0 1 0"
"1 0 0 1"
"1 0 0 0"
"[0 1 1 1]1 1 1 1"
"[0 1 1 0]1 1 1 0"

Again, ignoring the LSB, it can be seen that the above sequence consists of a decrementing count, and that the column address for each pair of addresses is the same for both the even and the odd addresses in each pair.

Paragraph beginning at line 26 of page 9 has been amended as follows:

In the interleave mode, the correct sequence of column addresses for a starting column address of "1 0 1 1" is as follows:

"1 0 1 1"
"1 0 1 0"
"1 0 0 1"
"1 0 0 0"
"[0 1 1 1]1 1 1 1"
"[0 1 1 0]1 1 1 0"

"[0 1 0 1]1 1 0 1"

"[0 1 0 0]1 1 0 0"

Again ignoring the LSB, it can be seen that the above sequence consists of a decrementing count in which the bits toggle correctly for an interleave sequence as explained above, and that the column address for each pair of addresses is the same for both the even and the odd addresses in each pair.